REMARKS

The Office Action mailed July 13, 2004 has been carefully reviewed and the forgoing amendment and following remarks are made in consequence thereof.

Claims 1, 3, 5, 6, and 26-30 are pending in this application. Claims 1, 3, 5, 6, and 26-30 are rejected. Claims 2, 4, and 7-25 have been canceled.

The rejection of Claims 1, 3, 5, 6, and 26-30 under 35 U.S.C. § 112, first paragraph is respectfully traversed. Applicant respectfully submits that the Section 112 rejection is based on the assumption of a temporal sequential order that is not claimed nor described in the present specification. Rather, in contrast to the Section 112 and as shown in the Figures and described in the specification, at least some of the elements of Claims 1 and 26 may occur concurrently, or in a temporal order that is different than the order listed in Claims 1 and 26. For example, in a logic circuit some signals may race and affect a logic output depending on which signal arrives at the next logic gate first. This phenomenon may be due to the inherent electrical characteristics of some circuit components. For example, as shown in Figure 3, Set Override-Reset and Delay Initiation logic may be used to coordinate logic signals to facilitate determining a predetermined logic output even though logic signal inputs may arrive at certain logic gates at different times. Moreover, Applicant respectfully submits that one skilled in the art, after reading the specification, in light of the Figures, would understand that the elements of Claims 1 and 26 may occur concurrently and/or in a temporal order that is different than the order they are listed in the Claims, and as such there is no requirement to list claim elements in a temporal order when no temporal order exists or when a temporal order may vary based on inherent circuit or process characteristics. Applicant respectfully submits that Claims 1, 3, 5, 6, and 26-30 satisfy the requirements of section 112, first paragraph.

Accordingly, for at least the reasons set forth above, Applicant respectfully requests the rejection to Claims 1, 3, 5, 6, and 26-30 under section 112, first paragraph be withdrawn.

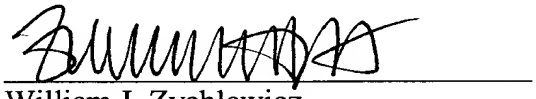
The rejection of Claims 1, 3, 5, 6, and 26-30 under 35 U.S.C. § 112, second paragraph is respectfully traversed. As described above, Applicant respectfully submits at least some of the elements of Claims 1 and 26 may occur concurrently or in a temporal order that is different than the order listed in Claims 1 and 26. For example, Claim 1 recites, "initiating a

predetermined time delay...resetting each of the plurality of operating modes during the time delay...switching the system to a second operating mode without going to a standby mode." As described in the specification and illustrated in Figure 3, the same mechanism that initiates the predetermined time delay also may initiate other concurrent actions and expiration of the time delay and/or the other concurrent actions also may initiate the switching of the first mode to the second mode. Applicant respectfully submits that one skilled in the art, after reading the specification, in light of the Figures, would understand that elements of Claims 1 and 26 occur concurrently and/or in a temporal order that is different than the order they are listed in the Claims and that elements of the Claims may initiate or be the cause of other actions that take place. Applicant respectfully submits that Claims 1, 3, 5, 6, and 26-30 satisfy the requirements of section 112, second paragraph.

Accordingly, for at least the reasons set forth above, Applicant requests the Section 112, second paragraph, rejections of Claims 1, 3, 5, 6, and 26-30 be withdrawn.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,



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